

DESIGN FOR PACKAGEABILITY: AN OVERVIEW

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ABSTRACT

To achieve higher performing systems, microelectronic system designers should consider the effects of packaging while developing integrated circuits (ICs). This practice, which we call "Design for Packageability", should permit a global optimization of the entire system by incorporating critical packaging factors into the IC design flow. Managers and engineers must be able to perform an early analysis of the expected system performance and cost prior to committing major engineering resources and capital to its development. Early analysis computer-aided design (CAD) software is being developed to show the effects of various IC design alternatives which may have even more impact on overall system performance than the change from conventional packaging to multi-chip module (MCM)-based packaging.

INTRODUCTION

For several years, the development of higher performing supercomputers spurred IBM to develop MCM technology which uses ICs with area pads. The bonding procedure used by IBM is known as C4 (controlled-collapse chip connection) in which pads may be located within the area consumed by the IC and not just on its periphery. Not only do area pads provide the IC designer with more I/O, and hence increased bandwidth when communicating with other ICs on the module, but it also increases the testability of the IC while reducing its size, power consumption and cost. Now that IBM and others are making this MCM-based technology available to non-IBM designers, there is a need for IC designers to alter their mind-set to design ICs which use area pads. Thus, new trade-offs will be presented to the IC designers and these changes in packaging technology should be incorporated into the CAD tools that the IC designers use.

This specific example falls within a larger class of design which we have chosen to call "Design for Packageability".

Just as the practice of Design for Testability resulted in overall better systems, we believe a similar impact can be made by following this procedure in the case of MCM-based systems. Until Design for Testability was followed, many IC designers made trade-offs which resulted in almost impossible problems for test engineers to solve. By incorporating a few features early in the design process, the resulting ICs were more easily and readily tested. This same result should be experienced with Design for Packageability in that a more globally optimum system should be developed if IC designers think ahead and make trade-offs with critical packaging parameters in mind.

Moreover, this concept can be extended to the general problem of performing optimization on separate domains such as design and technology. If each domain is treated in isolation, then suboptimal systems will result. Whereas treating a proper mix of the domains simultaneously can lead to globally optimum systems.

In this paper, we first present some preliminary results of applying the Design for Packageability methodology. The specific case considered is the impact of bonding technology on the overall system performance. Next, the goals of our research project will be described as a means of proving and advancing this methodology. Finally, conclusions are presented to indicate the importance of this work.

THE NEW METHODOLOGY

The design flow for this new methodology can be visualized as shown in Figure 1. In the past, IC designers have designed their chips thinking that each one would be housed in a single package and then interconnected on a printed circuit board (PCB). With the availability of MCM technology, system designers are initially taking the same chips (or not changing the traditional design flow) and packaging them in an MCM. The expected increase in system performance is generally achieved since the large capacitances involved in driving traces on a printed circuit board have been removed

and the number and density of the interconnections have improved dramatically.

However, following this traditional design flow does not fully exploit the capabilities of the MCM technology. Only when the IC designer realizes the potential advantage of designing his chips for the bonding that is available in the new technology is the system fully optimized.

For comparison purposes, consider three systems as illustrated in Figure 2. System 1 consists of peripheral-pad ICs which are wire-bonded onto a conventional PCB substrate. This serves as an example of today's typical systems. A normalized performance factor of 1.0 (i.e. a measure of power, size, speed, etc.) is assumed for this system for comparison purposes. System 2 (following the traditional design flow) utilizes the same set of ICs. Hence, these ICs are wire-bonded onto a MCM substrate. This is representative of the second class of systems that is being widely used as a quick boost in system performance by moving from a PCB to a MCM. The gain in the performance is completely due to the change in substrate. An assumed value of 20 % is shown in Figure 2.

Following the new design for packageability methodology, the third system consists of a new set of area-pad ICs which are C4-bonded onto a MCM substrate. Calculations indicate that System 3 will outperform the other two systems because of the change in the integrated circuits. A representative value of 30 % is shown in Figure 2.

Published reports indicate that this new methodology is not currently being practiced. Reports in the literature can be divided into two areas: experimental and global. The experimental results show the impact of packaging by fabricating a system based on two or more packaging techniques [1, 2]. They compare conventional packaging with MCM-based packaging. The ICs (dies) remain the same in either package and all comparisons are done at the system level. No formal discussions are given and the change in the system performance is due completely to the change in the packaging environments.

The global results reported to date include SUSPENS, AUDiT, and MSDA-PKG [3-5], which use formal discussions to describe the impact of packaging. They approach the issues by using a mathematical model to describe the system in terms of the package and the ICs. This model is then used to describe the impact of the packaging in the overall system performance. The packages are described by their physical and electrical characteristics. The ICs, however, are modeled globally by the physical sizes of the dies and the number of I/Os.

All of the above tools consider only the effect on system performance provided by the package. None of these methods takes into account the impact of the die on system performance. They all assume that the performance of the die is independent of the choice of packaging.

Recent work by the Microelectronic Systems Group at the University of Tennessee has investigated the effect on system performance of the die for two different packaging technologies [6]. As a proof of principle, an image processing chip-set was designed based on the Massively Parallel Processor (MPP). This chip-set was designed, simulated, and synthesized for conventional peripheral pads (wire-bondable) and for area pads. The preliminary results demonstrated how the performance of the dies change as a result of changes in the design being targeted for peripheral pad bonding and area pad bonding. The impacts of the packaging technolo-

gy on the performance of the dies have been demonstrated quantitatively in the following areas: power, size, testability, and cost. In the case for size, the effect of the package on system performance was 21 % and the effect of the die was 20 %. Evidently, changing only the package did not result in an optimum system. It took a change in the design of the IC to achieve the full benefits of the new MCM-based technology.

SYSTEM OPTIMIZATION NEEDS

In light of the potential this methodology has for enhancing the overall system performance of MCM-based systems, a variety of needs become apparent. These include:

1. MCM-based system optimization should be investigated, demonstrated and documented primarily by incorporating critical packaging factors into the design of the integrated circuits.
2. The procedure for using area pads rather than peripheral pads should be utilized, documented and promulgated publicly as part of a Design for Packageability Procedures Manual.
3. A comprehensive system model that can be used to analyze and compare from a system designer's viewpoint the impact of different packaging technologies and different IC design methodologies should be developed.
4. The effect on system performance and cost of changing from PCB-based to MCM-based packaging should be demonstrated.
5. Similarly, the effect on system performance and cost of changing from ICs using peripheral pads to those using area pads should be demonstrated using two MCM-based systems.
6. Early analysis CAD software incorporating such a system model should be developed and made available to others.
7. Return on investment calculations should be made to assist managers and engineers in deciding when it is appropriate to use area pads rather than peripheral pads.
8. Commercial CAD software for designing ICs should be enhanced to include consideration of critical packaging parameters.
9. Seminars and short courses should be organized to disseminate the results of these studies and demonstrations.

Portions of the above tasks are presently being undertaken by a team of researchers at the University of Tennessee, SUN Microsystems and MCC. Conventional approaches to microelectronic system design, partitioning and physical IC design will be optimized to take full advantage of MCM packaging. The purpose of this project, which is sponsored by the Advanced Research Projects Agency, is to assist the system designer in exploring the design space in order to perform this optimization. This goal will be accomplished by identifying the areas of the design cycle which benefit the most from exploiting the new opportunities which MCMs provide.

In support of these objectives, the following will be developed:

1. Early Analysis Tool: This tool will allow the system designer to explore IC and package options at an early stage of the design which may be input at different levels of abstractions including conceptual, behavioral and structural representations.
2. Simultaneous IC and MCM Physical Design Tool: This interactive tool will enable the system designer to consider the placement of the ICs on the MCM substrate before completing the IC pin assignment and physical design.
3. Optimized Partitioning Tool: This tool will partition a given design at different levels of abstractions. It will differ from other partitioning tools in that it will consider salient features of the chosen MCM technology.
4. Multi-objective Design Advisor: This information management tool will empower the designer with an efficient way of analyzing results and performing trade-off studies.
5. Application of Design for Packageability: The tools described above will be utilized to analyze and partition an industrial-strength system (SUN MicroSparc CPU) into multiple ICs that will be fabricated and tested as a single MCM.

CONCLUSIONS

Multi-chip integration technology has the potential to increase significantly overall system performance and reliability while reducing size, weight, power and cost. The work described here explores and demonstrates the impact of these MCM-based technologies on IC design and, hence, on the overall system. Development and verification of the planned Design for Packageability procedures should accelerate the architectural exploitation of both ICs and MCMs and result in higher performing systems.

Armed with this knowledge, system designers could answer the following types of questions:

1. What are the costs and benefits of using area pads instead of peripheral pads when designing ICs to be packaged in a MCM?
2. What architectural changes might be made that would result in significant enhancements in system performance and cost?
3. Is it worthwhile to redesign existing peripheral pad ICs to be area pad ICs?
4. What changes need to be made to commercial CAD software to include these critical packaging factors?

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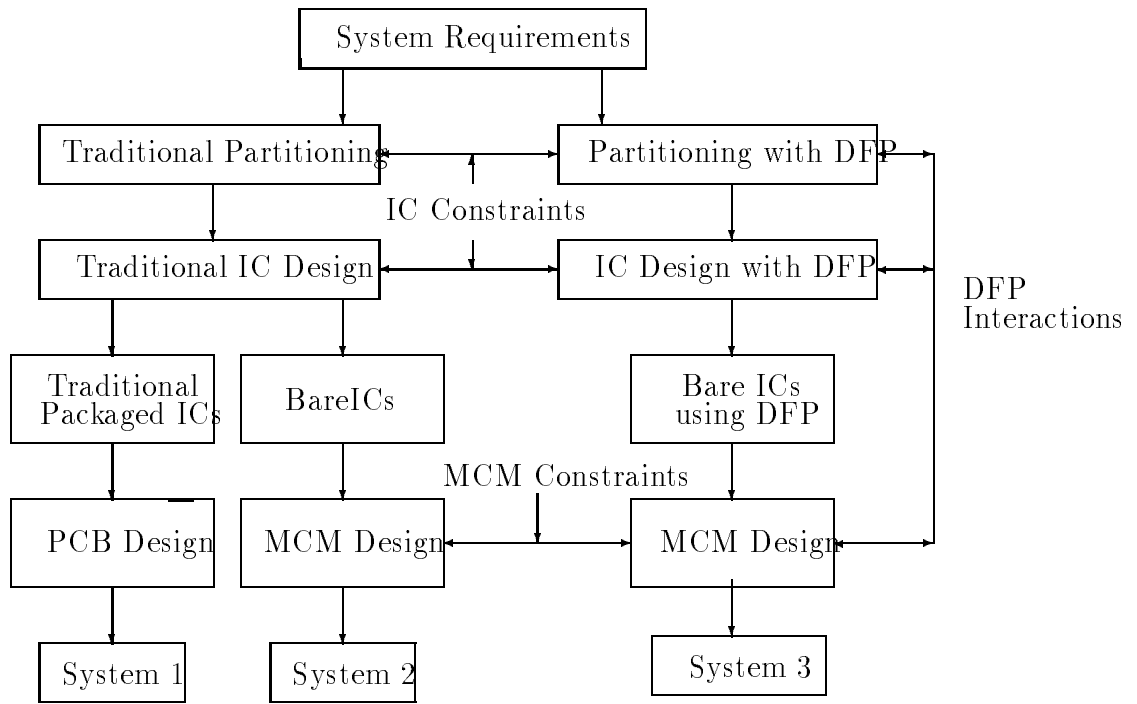


Figure 1: *Design for Packageability Methodology.*

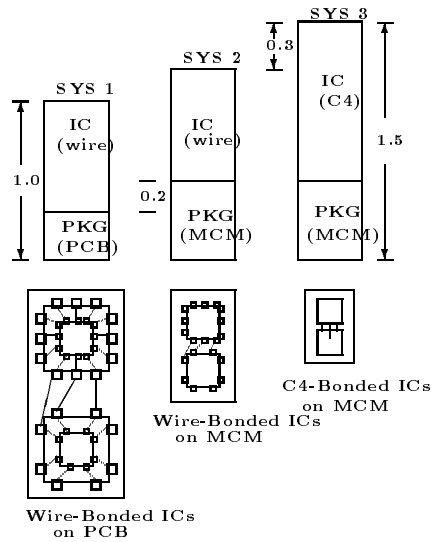


Figure 2: *Change in System Performance due to Package and IC changes.*