

# PERFORMANCE COMPARISON OF MCM-D AND SMT PACKAGING TECHNOLOGIES FOR A DSP SUBSYSTEM

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## ABSTRACT

*Advanced packaging technologies such as MCMs offer superior performance as compared to the conventional PCB technologies. This paper discusses the design, development, and comparison of a general-purpose programmable DSP subsystem packaged in MCM and conventional surface-mount technologies. The subsystem contains a 32-bit floating-point programmable DSP processor along with 256 K-bytes of SRAM, 128 K-bytes of FLASH memory, a 10 K-gate FPGA, and a 6-channel 12-bit ADC. The complete subsystem has been interconnected on a 37 mm by 37 mm MCM-D substrate and is packaged in a 320-pin ceramic quad flat pack. This paper evaluates electrical and thermal performance for the MCM-D substrate and compares the results with the SMT version of the design.*

## 1. INTRODUCTION

Today's sub-micron IC technologies have low-latency device characteristics that promote higher clock speeds than in the past. In high-performance systems, 50 percent of the total system delay is usually due to packaging and interconnect [1].

Advanced packaging technologies such as MCMs are emerging as a viable solution to this problem. Multichip modules provide housing and interconnect for multiple bare dies on a single high-density multi-layer substrate. Multichip module packaging has been in use by IBM and others for many years, but only recently has a low-volume and low-cost service become available to the design community [2].

As MCMs gain popularity, designers need to evaluate its cost/performance with the conventional technologies at the final system level to justify the insertion of such a technology. This paper evaluates the performance of a DSP sub-system based on MCM-D and surface-mount (SMT) technologies. The results (electrical and thermal) as well as technology descriptions are included in the

following sections. The paper concludes with a discussion on MCM related issues and conclusion.

## 2. FUNCTIONAL DESCRIPTION

The design is a DSP subsystem based on the Motorola 96002 32-bit programmable floating-point DSP processor. In addition, the module includes 256 K-bytes of SRAM, a 128 K-byte EEPROM, a 10 K-gate Xilinx 4010 FPGA, and a 6-channel 12-bit ADC. The module was designed to exploit the multi-processing capability of the 96002. The FPGA is primarily a hardware pre-processor of incoming data but also provides other generic logic functions required for implementation of the entire subsystem.

## 3. PACKAGING TECHNOLOGIES

Two packaging technologies have been evaluated: MCM-D and SMT. The characteristic of both technologies are shown in Table 1 and Table 2 respectively. The MCM-D substrate is a 37 mm x 37 mm 5-layer (1 pad, 2 power, and 2 routing layers) substrate based on the *MicroModule Systems Merged Via D500* process [3]. Copper is used for the routing layers and positive power plane, and a 50 mil aluminum substrate serves as a ground plane. The top layer is the pad and die connect layer. The die are attached to the thin film interconnect using epoxy and are wirebonded to pads using gold wire. For the top layer of metallization, no routing is allowed, and all pads have vias that connect to the appropriate signal layers or power planes. The MCM is packaged in a cavity-down, 320-pin ceramic quad flat pack with preassigned power and ground pins.

The SMT board is 6.5 inches long and 3.75 inches wide with 6 metallization layers (2 power planes and 4 trace layers). Two of the trace layers are on the PCB top and bottom surfaces and share area with the components. The remaining two trace layers are internal and sandwiched between the power planes. All metallization layers are standard 1 oz. copper, and the dielectric regions of the board are constructed using standard 10 mil FR-4 glass epoxy. In order to facilitate the high interconnect

demand for this design, buried vias are used to connect between layers. PCB is assumed to have characteristics as described by [4].

#### 4. ELECTRICAL ANALYSIS

Figures 1 and 2 show the final routed MCM and SMT layouts. Table 3 lists the area efficiency statistics of the MCM and SMT implementations. A complete detailed comprehensive analysis is presented in [5].

The entire design was simulated with *QUAD's XNS* tool [6] to identify the limitation of both technologies. Fast I/O driver models (rise and fall times of approximately 1 to 4 nsec.) were used to simulate all digital networks and I/O for both design representations. Several simulations were performed using drivers with unloaded rise and fall times ranging from 4 nsec to 1 nsec. Table 4 lists the worst case results for the simulations performed using 1 nsec rise/fall time drivers (limitation of the design without termination resistance).

The MCM-D substrate was found to be much faster than the SMT PCB. The decrease in net delay for the MCM-D can be attributed to several factors including the removal of single-package pin parasitics and reduced parasitic net capacitance. For PCBs, single-package pins contribute inductance and capacitance which can seriously distort and delay signals. When the bare die are placed on the MCM-D substrate, the single-package pin parasitics are replaced with wirebonds which have much less parasitic capacitance and inductance. In addition, the MCM-D interconnect traces are much smaller and shorter, and therefore, they contribute much less parasitic net capacitance.

The MCM-D was also found to have less crosstalk between traces than the PCB. The crosstalk was only calculated on the plane of the routed trace. Other routing planes which could cause contributions from intersecting traces were not considered. The reduced crosstalk for the MCM-D can be attributed to shorter segments of parallel traces and a reduced thickness in trace metal compared to the SMT PCB. Crosstalk is a result of capacitive coupling and inductive coupling between traces. By reducing the length of parallel trace segments, the mutual capacitance and inductance are reduced. In addition, the MCM-D traces are 4  $\mu\text{m}$  thick compared to the PCB trace thickness of 1.4 mil (35.6  $\mu\text{m}$ ). So, the effective area of potential coupling is also reduced.

Next, overshoot and undershoot measurements are considered. Again, for 1 nsec drivers, the MCM-D substrate resulted in improved signal performance. Overshoot and undershoot are directly related to driver rise and fall times and the characteristics of the network and receivers being driven. For the MCM-D version, the single-package pin parasitics have been removed, and the

traces are less capacitive. The result is a cleaner and better behaved signal as indicated in Figure 3. The results listed in Table 4 indicate that the SMT PCB would be border line to inoperable when using 1 nsec drivers because of overshoot and undershoot problems. Although the MCM-D values are slightly high, they are still within the acceptable operating range of all devices in the design.

Power distributions in both systems are compared in terms of supply bounce. Supply bounce is related to the inductance of the power distribution network. Supply bounce results when a large amount of current is passed through an inductive network in a very short time. Table 4 shows the simulation results for both MCM-D and SMT. These supply bounce simulations were performed with all possible drivers switching simultaneously and no decoupling capacitance was considered. The results which are Pessimistic (since no decoupling capacitances are included in the simulation) indicate that the MCM-D substrate will have less supply bounce than the SMT PCB substrate in worst case condition (driver with 1 nsec. rise time). For the PCB, the supply bounce is higher because of the parasitic inductance of the single-package pins. In single-package components, power/gnd pins on the package are inductive. In addition, multiple power and ground pads are often bonded to a single pin resulting in a high inductive path for current during signal transition. When bare die are placed on a MCM substrate, each pad can be bonded separately significantly reducing inductance resulting in lower supply bounce. Also, supply bounce can be reduced with the addition of decoupling capacitance. Decoupling capacitors can supply charge to drivers during simultaneous transitions when the inductance of the power network prevents large instantaneous current influx. For PCBs, it is considered routine procedure to include a significant amount of decoupling capacitors in cases where supply bounce could result. For the PCB design in this paper, decoupling capacitors occupy the bottom side of the SMT board. For the MCM-D design, there is an inherent low inductive decoupling capacitor (approximately 10 nF) present between the power and ground plane because of the construction of the MCM substrate.

#### 5. THERMAL ANALYSIS

MCMs integrate several large VLSI dies consuming several Watts within a small area. Thermal analysis of an MCM is very important to ensure a reliable operation. The objective of thermal analysis is to predict the junction temperature of the dies in determining long-term reliability of the components and the module. The results for the MCM and PCB were generated using three-dimensional finite-element mesh analysis at 25 °C in still

air. For the MCM-D, the thermal path from the die to heat sink is comprised of the following three paths:

- Path1 =  $R_{die} + R_{die\ epoxy} + R_{interconnect}$
- Path2 =  $R_{MCM\ package} + R_{interconnect\ epoxy}$
- Path3 =  $R_{thermal\ grease} + R_{heat\ sink}$

Thermal vias were placed under all the dies to improve the thermal conductivity path from the dies to the backing plate. Thermal vias were created in such a fashion to allow two traces between them. This resulted in less routing penalty under the dies due to the thermal vias. The thermal parameters and results for the MCM-D are listed in Table 5. The maximum junction temperature was simulated to be 50 °C at the FPGA which is well within the maximum rating of the dies.

The thermal parameters and results for the PCB are listed in Table 6. The simulations assumed no heat sink on any of the components. The maximum junction temperature was simulated to be 62 °C at the FPGA which is well within the maximum rating of the dies.

### 6. MCM-RELATED ISSUES

With the evolution of MCM technology, it is permissible for engineers to consider a design flow incorporating MCM technologies. This allows the designer to make better decisions concerning the physical implementation of the design. Early-analysis tools such as [7] offer designers quick comparisons of different packaging technologies for their specific application.

However, there are still problems in obtaining Known Good Die. These issues include potentially long lead times and small selection of bare die for a given design. More effort needs to be expended in the release of I/O driver simulation models (IBIS or SPICE) by the IC vendor to ensure proper simulation results.

With MCMs, testing can be a problem since the lines and pins are not easily probed. Therefore, design for testability (DFT) techniques must be incorporated from an early phase of the design. Using boundary-scan components can help with the testing; however, not all the components have boundary-scan capabilities.

### 7. CONCLUSION

Multichip modules are becoming a viable choice of packaging for high performance/miniaturized electronics. This technology is no longer considered to be an exotic technology and is being used in telecommunications, consumer electronics and workstations. MCMs offer superior performance as compared to the conventional technologies (packaged-part on PCB). An appropriate system-level cost/performance comparison (along with risk factor) of MCM with the conventional technologies

may justify the usage and insertion of such a technology. Availability of the bare dies (and their I/O buffer models) and testing issues will be challenging issues to be considered.

### REFERENCES

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- [5] Powell, T., "The Development, Design, and Comparison of Printed Circuit Board and MultiChip Module Representations of a DSP Subsystem", *Master's Thesis*, University of Tennessee, May, 1996.
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MCM-D SUBSTRATE CHARACTERISTICS	
Substrate Property	Value
Dielectric	Polimide
Dielectric Constant (Er)	3.5
Metallization	Copper
Copper Resistivity	1.7E-6 Ohms-cm
Number of Trace Layers	2
Number of Power Planes	2 (VCC and Ground)
Board Thickness	1.3 mm (52 mils)
Component Mounting	Wirebonded (Top Surface Only)
MCM-D TRACE CHARACTERISTICS	
Signal_1 Trace Property	Value
Width	20 um (42 um spacing; 62 um pitch)
Characteristic Impedance	58 Ohms
Capacitance	1.0 pF/cm
Inductance	3.4 nH/cm
Resistance	2.0 Ohms/cm
Propagation Delay	58 ps/cm
Signal_2 Trace Property	Value
Width	16 um (46 um spacing; 62 um pitch)
Characteristic Impedance	50 Ohms
Capacitance	1.2 pF/cm
Inductance	3.0 nH/cm
Resistance	2.4 Ohms/cm
Propagation Delay	60 ps/cm

Table 1. MCM-D Properties

SMT BOARD CHARACTERISTICS	
Board Property	Value
Dielectric	10 mil FR-4 Glass-Epoxy
Dielectric Constant (Er)	4.5
Metallization	1.4 mil Copper
Copper Resistivity	1.7E-10 Ohms-cm
Number of Trace Layers	4
Number of Power Planes	2 (VCC and Ground)
Board Thickness	60 mils
Component Mounting	Both Sides
SMT TRACE CHARACTERISTICS	
Surface Trace Property	Value
Width	8 mils (8 mil spacing; 16 mil pitch)
Characteristic Impedance	73 Ohms
Capacitance	0.767 pF/cm
Inductance	4.1 nH/cm
Resistance	23.5 mOhms/cm
Propagation Delay	56 ps/cm
Buried Trace Property	Value
Width	8 mils (8 mil spacing; 16 mil pitch)
Characteristic Impedance	55 Ohms
Capacitance	1.3 pF/cm
Inductance	3.9 nH/cm
Resistance	23.5 mOhms/cm
Propagation Delay	71 ps/cm

Table 2. PCB Properties

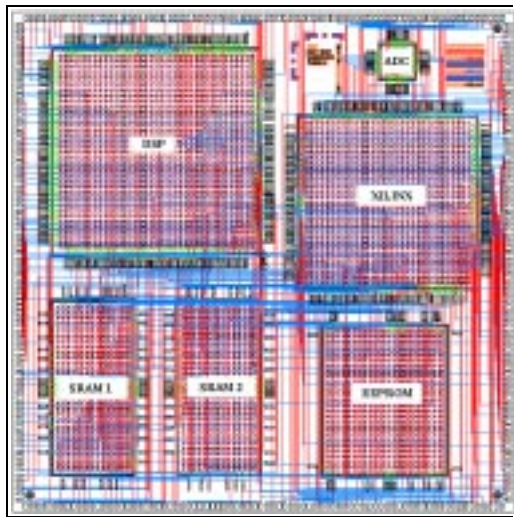


Figure 1. MCM-D Layout

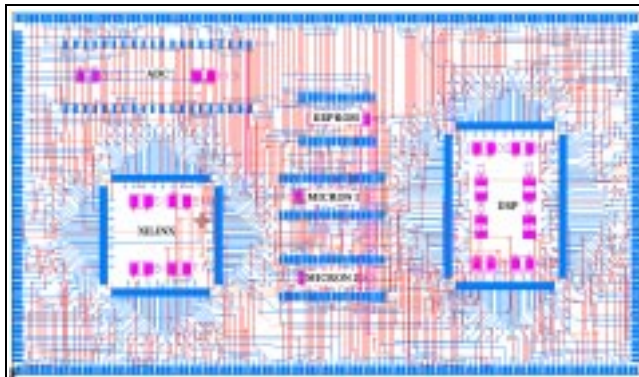


Figure 2. SMT PCB Layout

MCM-D COMPONENT DIMENSIONS				PCB COMPONENT DIMENSIONS			
Component	Width (mm)	Length (mm)	Surface Area (mm <sup>2</sup> )	Component	Package Width (mm)	Package Length (mm)	Package Surface Area (mm <sup>2</sup> )
DSP 96002	15	15	225	DSP 96002	28	40	1120
Xilinx 4010	12.88	12.61	162.42	Xilinx 4010	28	28	784.00
SRAM (2)	5.842	12.725	74.34	SRAM (2)	10.2	28.6	291.72
EEPROM	9.042	10.897	98.53	EEPROM	12.2	21	256.20
ADC	2.4	2.4	5.76	ADC	15	51	765
MCM-D SUBSTRATE	37	37	1369	SMT Board	95.25	165.1	15725.78
Total Chip Area (mm <sup>2</sup> )	640.39			Total Package Area (mm <sup>2</sup> )	3508.64		
Top Surface Area Efficiency (Chip Area/MCM Area)	46.78%			Chip Area/MCM Area	4.07%		

Table 3. Area Results

SIMULATION RESULTS					
	Net Delay	Crosstalk	Overshoot	Undershoot	Supply Bounce
MCM-D	1.44 nsec	214 mV	0.32 V	-0.23 V	0.65 V
PCB	5.0 nsec	479 mV	0.62 V	-0.59 V	1.4 V

Table 4. Simulation Results

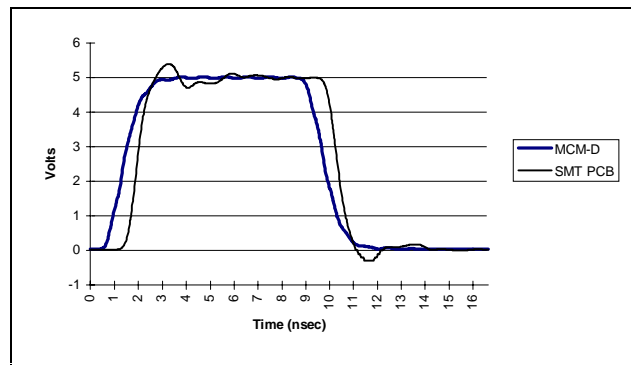


Figure 3. MCM and SMT PCB Signal Waveforms

MCM-D COMPONENT TEMPERATURES				
Component	Temperature Results (Celsius)			
	Minimum	Maximum	Average	Junction
DSP 96002	46.5	49.3	47.9	48
Xilinx 4010	47.2	49.5	48.3	48.3
SRAM (1)	45.5	47.7	46.6	46.6
SRAM (2)	46.6	48.5	47.4	47.4
EEPROM	44.5	47.1	45.8	45.8
ADC	46	46.2	46.1	46.1

Table 5. MCM-D Thermal Results

PCB COMPONENT TEMPERATURES				
Component	Temperature Results (Celsius)			
	Minimum	Maximum	Average	Junction
DSP 96002	56	59.9	58.9	59
Xilinx 4010	56.3	61.7	60.5	60.7
SRAM (1)	57.8	60.4	59.7	59.9
SRAM (2)	57.9	60.6	59.7	60
EEPROM	50.8	53.2	52.5	52.6
ADC	42.5	46.8	44.5	44.5

Table 6. PCB Thermal Results