Impact of Packaging Technology on System Partitioning: A Case Study

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Abstract

This paper emphasizes concurrent consideration of the partitioning of a microelectronic circuit design into multiple dies and the selection of the appropriate packaging technology for implementation of the entire system. Partitioning a large design into a multichip package is a non-trivial task. Similarly, selection of the MCM packaging technology to accommodate a multichip solution can also be puzzling. The interdependencies of these two problems afford the opportunity to achieve a global optimum when considered concurrently. In this paper we address the partitioning/MCM technology tradeoff, their interdependency, and previous work in this area. The SUN MicroSparc CPU is used as a demonstration vehicle and is partitioned for different MCM technologies. The preliminary results show that the optimum number of partitions and contents of each partition depend heavily on the choice of MCM technologies for a given application.

1 Introduction

Multi-chip modules have been gaining popularity and becoming more available during the past few years. The designer is now faced with a variety of MCM packaging technologies and has to understand and compare them for a given application. Conventionally, this has been performed by the package designer mainly toward the end of the design cycle. However, to achieve a more nearly optimum system, packaging-related issues **should be** considered throughout the design cycle by system, IC, and package designers. About 40% of the the product cost is determined by the decisions made in the first 10% of the design cycle [1]. This suggests that the choice of packaging should be explored at the early stages of the design for a more globally optimum system. Considering the critical packaging issues early in the design cycle is termed "Design for Packageability" (DFP) and is discussed in [2].

Comparisons between different MCM technologies cannot be made by just considering the physical and electrical parameters of the technologies. True comparisons should be made at the system level by understanding the impact of the different MCM technologies on the overall cost/system performance of the final system.

2 Problem Definition and Motivation

As a part of our research, we are trying to identify the stages in the design cycle which will benefit the most from taking advantage of the new solutions offered by MCM packaging. Figure 1 shows how partitioning drives all the system performance parameters such as system cost, size, thermal, power, packaging delay and simultaneous switching noise. Chip bonding and substrate technologies determine the physical constraints on the partitioning process. It can be seen that the choice of the packaging technology propagates through the partitioning process and then impacts system performance. Thus, there is a need to explore the effect of the various packaging technologies on system partitioning and hence system performance to achieve an optimum system. The main objective of our work is to study the interaction and impact of the various bonding and substrate technology alternatives on system partitioning and performance. Partitioning an ultra-large single die into multiple smaller dies housed on a MCM is used as an example; however, this approach can be applied to a larger class of applications using multiple levels of packaging hierarchy.

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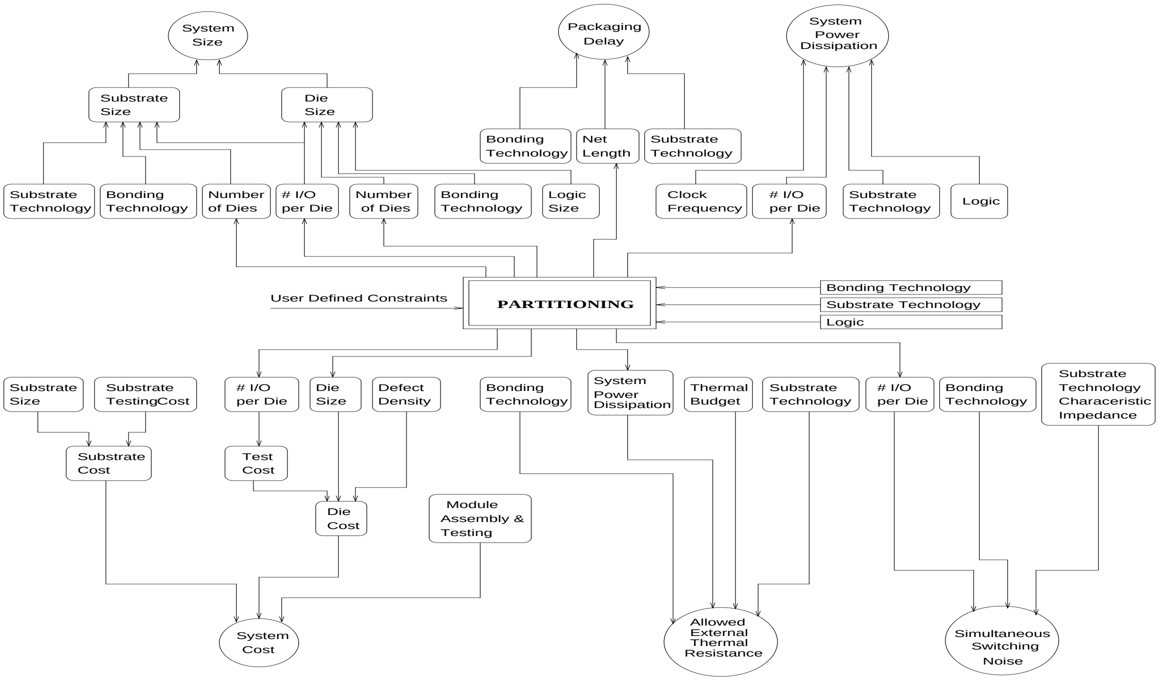

Figure 1: Interaction between System Performance Parameters and Partitioning using DFP.

The impact of bonding technologies such as area array (Flip-Chip, FC) and peripheral (Wire-Bond, WB) on the die size and layout of VLSI dies is discussed in [3]. That work was focused at the the physical die layout level rather than the system level. A more conceptual trade-off analysis between peripheral and area array bonding in MCMs is presented in [4]. The design is described in terms of gate counts used Rent's rule to establish the number of I/Os for a given circuit size. Our work tries to establish the interaction of the various packaging alternatives, partitioning and the system performance when more information is available about the design. The SUN MicroSparc is used as a demonstration vehicle to illustrate the extent of the interaction. The design is described at the functional unit level consisting of the following: integer unit (IU), floating point unit (FU), memory management unit (MMU), data cache (D-CACHE), instruction cache (I-CACHE), S-bus controller (S-BUS-CTL), memory interface unit (MEM-INTF), clock control and buffers (CLK-CTL), and miscellaneous control logic (MISC) as shown in Figure 2.

3 Approach

The intent of this work is not to promote a new partitioning scheme since numerous techniques have already been described [5],[6]. Our approach is to develop a framework in which various packaging/partitioning choices can be explored and evaluated concurrently. Since performing a detailed evaluation at the system level for various packaging/partitions can turn into a time-consuming task, we have employed an estimation-based, early-analysis technique. At this level there are only nine functional units so the number of possible candidates is low enough (approx. 21,000) that it is possible to search the solution space exhaustively. This guarantees the best solution will be found. At the register transfer level where there are a large number of components, it is more appropriate to use partitioning techniques based on algorithms such as simulated annealing which can guarantee a good solution among several possible solutions.

The steps involved in our concurrent analysis are shown in Figure 3. The user specifies the package and die related information (i.e. bonding technology, maximum die size). The constraint generator derives the actual constraints from these user specifications. The exhaustive partitioner then generates all possible candidate partitions. The algorithm used to generate partitions is described in [7]. The die size and die I/O estimates are then calculated for each of the partitions. Next the partitions are verified against the constraints. These constraints are used to qualify a partition for further processing. Further processing involves estimating the system performance characteristics such as system cost, system size, module power, allowed external thermal resistance and total simultaneous switching noise in the module. The MSDA (Multichip System Design Advisor) tool developed by MCC is used to estimate the system performance characteristics.

4 Results

We have concurrently considered the following:

a) Wire-Bond/MCM-C
b) Wire-Bond/MCM-D
c) Wire-Bond/MCM-L
d) Flip-Chip/MCM-C
e) Flip-Chip/MCM-D
f) Flip-Chip/MCM-L

The exhaustive partitioner has generated over 21,000 partitions for each type of packaging but only those partitions that meet the die and package constraints have been considered for analysis. The die parameters provided by the user are given in Table 1.

Property	Value
Signal/Ground (peripheral)	4
Signal/Ground (area array)	6
Bond pad size (peripheral)	200 * 200 (microns)
Bond pad size (area array)	125 * 125 (microns)
Min Bond Pad pitch (peripheral)	200 (microns)
Min Bond Pad pitch (area array)	250(microns)
Wafer Diameter	6 inches
Unusable Wafer Border	0.4 inches
Wafer defect density	3 defects per sq.inch
Processed Wafer cost	$800
Wafer Bumping cost	$200
Defects due to Wafer Bumping	0.2 defects per inch
Die Test cost	$0.01 per I/O

Table 1: Die Assumptions Provided by the User.

The result of the cost analysis is shown in Figure 4(a) which displays those partitions satisfying the given constraints with the lowest system cost for a particular number of dies in the die set. The FC/MCM-D design offers the lowest overall system cost for implementing this particular application in a MCM. The system cost is comprised of the die, bonding, substrate and assembly cost. The substrate and assembly cost estimates used in this analysis is discussed in [4]. The flip chip design offers higher I/O count and takes full advantage of the higher interconnect density of the MCM-D. The combination of these two choices reduces the die area (and hence the die cost) considerably as compared to the conventional peripheral wire-bond design. It should be noted that FC/MCM-D is not highly sensitive to the number of chips in the partition.

The multichip design implemented in WB/MCM-C and WB/MCM-D exhibit the highest overall system cost. The lower I/O count offered by the peripheral wire-bond design results in larger die area which results in reduced yield and higher die cost.

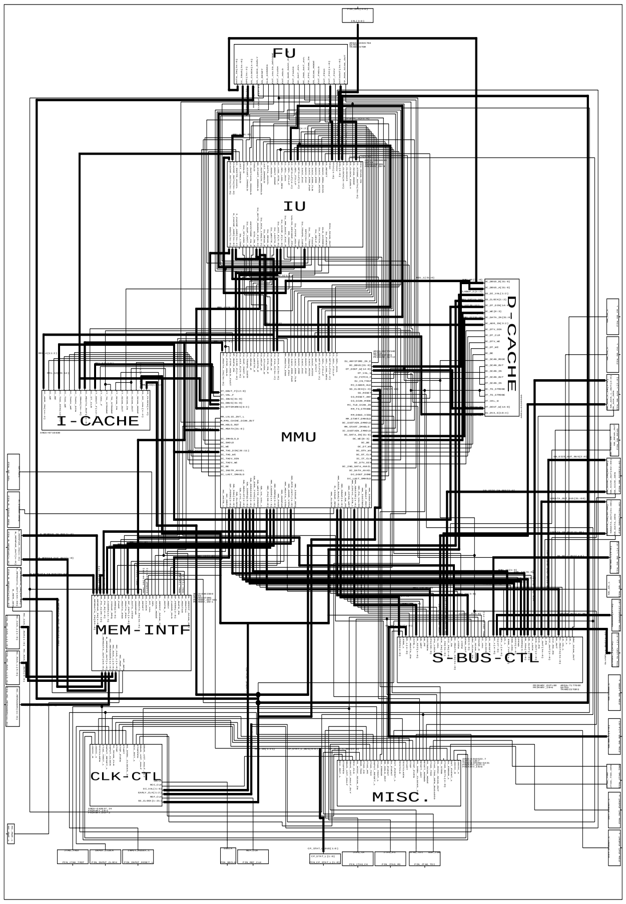

Figure 2: Functional-Level Diagram of the MicroSparc.

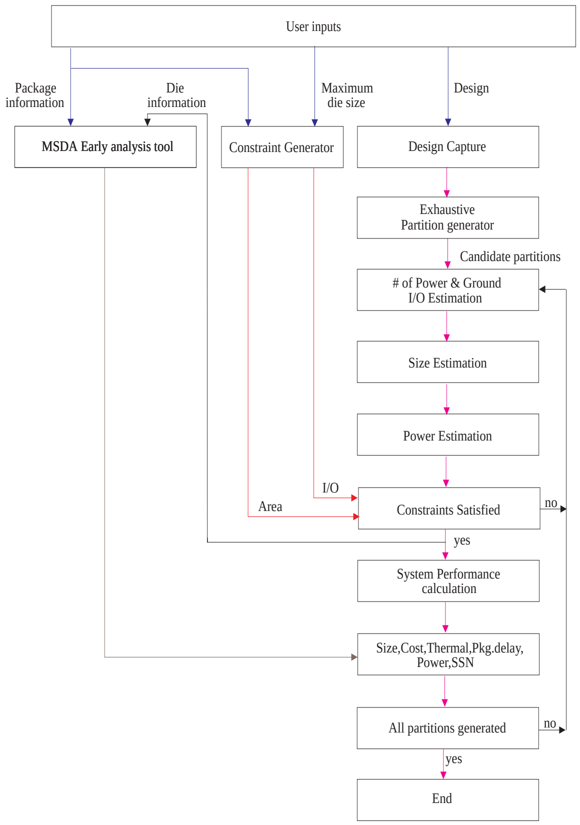

Figure 3: Block Diagram of Exhaustive Partitioning.

For this application, the die cost in the wire-bond case dominates the substrate and assembly costs. Therefore, the die set which offers the lowest system cost is the same for wire-bond design using any of the three substrates. However, this is not true for the flip-chip designs since the their die costs are comparable to the substrate and assembly costs.

Figure 4(b) shows the size of the partitions which offer the lowest system cost. The flip-chip design using MCM-D exhibits the smallest module size. This is due to the combination of the reduction in die area because of area-array bonding and the reduction in substrate size with the use of MCM-D interconnect.

A measure of the simultaneous switching noise analysis is shown in Figure 4(c). The noise data shown corresponds to the partitions having the lowest system cost. The flip-chip designs have lower inductance and hence provide lower switching noise.

Figure 4(d) shows the total power dissipation of the modules which have the lowest system cost. The flip-chip/MCM-D designs have higher power dissipation compared to the wire-bond designs since the flip-chip designs have more I/Os. The flip-chip/MCM-C has the worst power dissipation due to the higher interconnect capacitance of the substrate. In this particular application, the power dissipation increases with the increase in number of chips due to the increase in the number of outputs in the die-set.

The results from the thermal analysis is shown in Figure 4(e). The worst-case external thermal resistance of the die in the partition is heavily dependent upon the total power dissipation in the module. Higher values of external thermal resistance indicate less power dissipation inside the MCM. Thus, the external thermal resistance decreases with the increase in the number of chips in the partition. There are some versions of flip-chip/MCM-D where special process techniques (e.g. potting and lapping the completed assembly) result in better external thermal resistance characteristics.

Figure 4(f) shows a figure-of-merit for packaging delay of these MCM systems. The delay was computed for a length equal to the diagonal length of the module. The interconnect line was modeled as either lumped RLC or a transmission-line based on their lengths. Each line was terminated and a total of eight receivers were assumed for each driver. The delay calculations include time-of-flight, RC charging and reflections and, therefore, are a function of the dielectric constant and size of the MCM module. For the monolithic case, the delay was calculated for an interconnect signal line within the die with a length equal to the diagonal length of the die.

5 Summary and Conclusions

Each type of MCM technology has a different cost/performance characteristic. It is important to evaluate these technologies for the specific application in hand for the best price/performance. Evaluation and selection of these technologies should not be solely based on the physical and electrical characteristics of the technology itself but should be based on price/performance of the entire system by considering the interdependency of MCM technologies and partitioning at the system level.

The performance parameters of cost, size, power, thermal, simultaneous switching noise and package delay for the six different packaging alternatives are shown in Table 2. The candidate ranking was arrived by considering an overall figure of merit of the various

	Monolithic	WB MCM-L	WB MCM-C	WB MCM-D	FC MCM-L	FC MCM-C	FC MCM-D
System Cost ($)	400.05	330.70	365.17	364.94	147.46	66.18	57.45
System Size in^2	0.3488	1.34	1.34	1.34	0.9	0.91	0.6
Module Power (W)	4.9	5.0579	5.1162	5.0388	5.1946	5.7227	5.6963
Ext. Therm. Res. (degC/W)	12.69	11.45	11.05	11.59	10.52	8.06	9.63
SSN	124	410	494.17	476.03	6.85	8.07	7.77
Pkg. Delay (ns)	0.7918	1.3229	2.1792	1.3806	1.2134	1.9289	1.1459
Ranking		4	6	5	2	3	1

Table 2: Comparison of System Parameters for Bonding and Substrate Technologies.

Chip	Pins	Area (mm^2)	Modules
1	485	49.428059	D-CACHE, I-CACHE, MMU
2	298	45.510590	FU, IU
3	414	28.451555	MEM-INTF, SBC, CLK-CTL, MISC.

Table 3: Contents of the Best Overall Partition.

system performance parameters. The best partition, consisting of three dies, is shown in Table 3.

For this particular application, the results indicate that the overall system cost would be reduced by a factor of seven if the single-chip CPU were divided into three chips, bonded using flip-chip technology and interconnected on an MCM-D substrate.

To date, the functionality of the partitions has not been considered by the partitioning tool. There is still a need for an experienced system architect designer to compare the results for the best design architecture. We plan to analyze the cost/performance of the different cache sizes added to the design and perform the detailed analysis of the above candidate designs to verify the validity of the model used in the analysis.

The methodology of partitioning with DFP in mind is applied here to a design described in the functional unit level. We plan to extend this concept to designs described at the behavioral and structural (RTL) levels as well.

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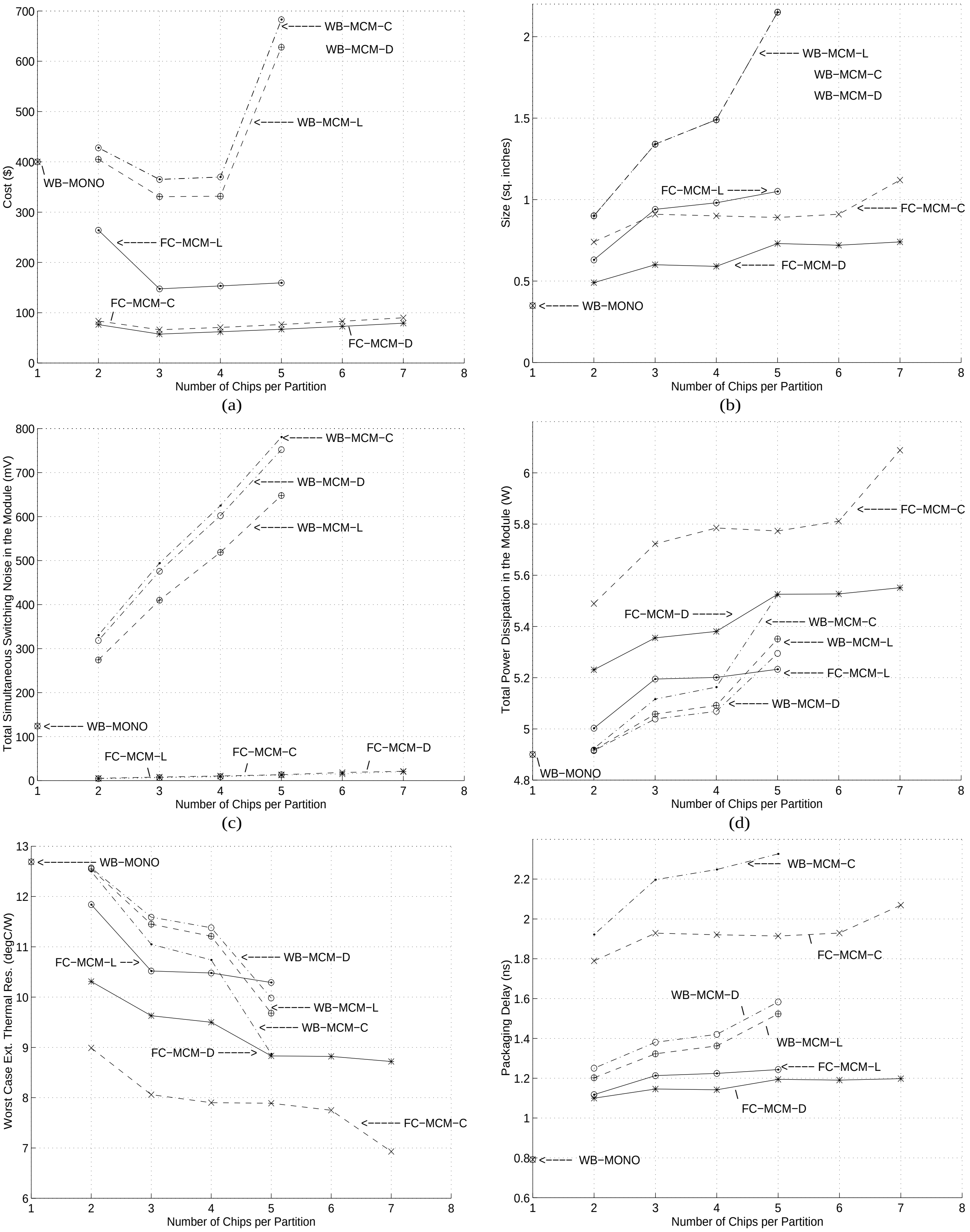

Figure 4: Results of the System Performance Analysis.