Determination of Area-Array Bond Pitch for Optimum MCM Systems: A Case Study

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Abstract

Microelectronics system designers need to understand and evaluate the impact of advanced packaging parameters which have become an integral part of microelectronics systems. This paper evaluates the impact of bond pitch for a flipchip multichip system through a case study. The SUN MicroSparc CPU was used as a representative of a large design where the design has to be partitioned and interconnected using MCM technology. Early analysis techniques were used to analyze the design for various pitches ranging from 150 to 400 micron in 50 micron increments. Results suggest that various bond pitches affect the system cost/performance and there is a minimum pitch at which lowering the pitch will degrade the cost/performance metrics.

Introduction

Optimization of microelectronics systems continue to be a difficult task since it involves a number of different disciplines. Since advanced packaging technologies are an integral part of high performance microelectronics systems, the optimization process becomes even more difficult. The system designer is now faced with dealing with the packaging issues as well as other traditional issues.

Traditionally, packaging selection and evaluation is done by the package designer within the limit of the packaging technology itself. However, some of these parameters have an impact at other phases of the design which may impact the system optimization. Therefore, it is important to identify some of these parameters and evaluate their impact for a given application at the system level to obtain optimum system design.

Bond pitch of a flipchip/MCM system is one of the important packaging parameters which can impact other phases of the design (i.e. IC design and partitioning). This paper will evaluate the impact of the bond pitch at the system through a case study. In the following sections, the relationship between the bond pitch and other system parameters will be identified. The SUN MicroSparc CPU will be presented as a case study along with the results and conclusions.

Flipchip Bonding Technology

Area array bonding technologies such as flip-chip (these two names are interchangeably used throughout this paper) are gaining more popularity with the advancement in packaging technologies. Flipchip technology is expected to grow at a compound annual growth rate of 38% through the year 2001 [1]. This technology offers higher I/O count for a given die size as compared to the conventional wire-bond technology. This is due to the placement of the I/O pads on the area of the die rather than just on the periphery as shown in Figure 1. Therefore, the total I/O count is a function of the square of the die size and the bond pitch.

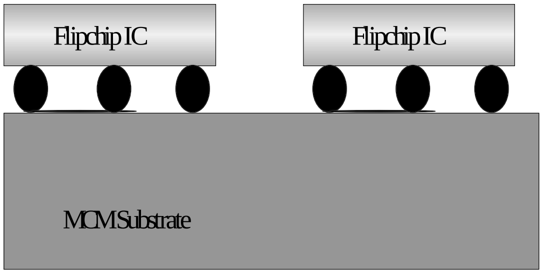

Figure 1. Flipchip Dies on MCM Substrate

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Theoretically, from an IC point of view, decreasing the bond pitch (assuming manufacturing is possible) will result in a higher number of I/O for a fixed die area. However, from the substrate designer point of view, one has to be concerned with the "escape routing" of these pads as shown in Figure 2. In this paper, escape routing is referred to the routing of the area-array I/O pads from the area under/surrounding the die to the vias (for redistribution to other layers) or the top layer routing on the substrate. As explained in [2], the upper bound for the number of I/Os which can be **placed** on a die and **escape routed** is a function of the die size (determined by the IC technology), bond pitch (determined by the bonding technology), and the wiring pitch on the substrate (determined by the substrate technology). This upper bond density (number of I/O per unit area) is provided by [2]:

$$N = \frac{b^2}{4}\left(-1-\sqrt{1+\frac{4}{b}}\right)^2 \qquad (1)$$

$$b = -\frac{4(P_{top}+1)(2+S{:}G)-8}{S{:}G} \qquad (2)$$

Where:

N is the total number of I/O that can be escape routed

P_{top} is number of tracks allowed between I/O pads

S:G is the signal to ground ratio assuming equal number of power and ground

IC designers are usually faced with a high I/O requirement for their single chip designs. High I/O also impacts the partitioning boundaries of a multichip design (i.e. large design into smaller designs). Area-array bonding can offer a high I/O if the chip is designed specifically for area-array technologies (i.e. not a re-distribution of the periphery I/Os)[3]. For a globally-optimum system design, it is important to consider not only the I/O requirements at the IC level but also the escape routing requirements at the package level which in turn drives the partitioning boundaries in a multichip design. This requires understanding the interaction between the IC and the package at the system level and how to optimize the system accordingly.

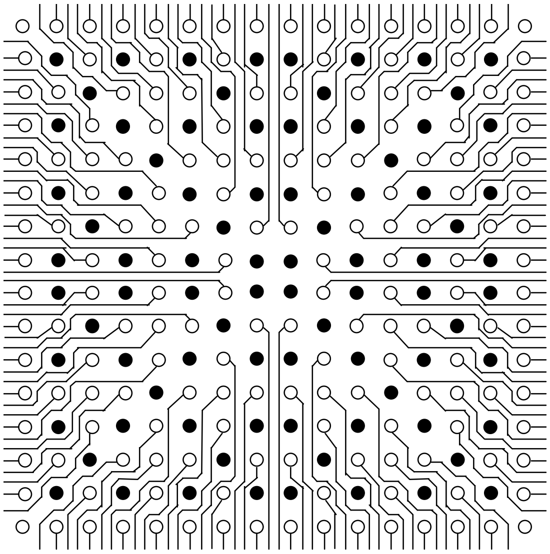

Figure 2. Possible Escape Routing from a uniform 16x16 Area Array Bond Pads. Shaded Points are Power and Ground I/Os [2].

Case Study and Results

In our previous work [4], we have proposed the concept of design for packageability (DFP) in which the packaging issues are considered at an early stage of the design for an optimum MCM solution. This concept was used to predict the cost/performance for a large design (SUN MicroSparc CPU) which was partitioned into smaller area-array dies and re-interconnected on an MCM-D[5]. This paper extends the previous study by considering the impact of the bonding pitch for the MicroSparc application.

We evaluated a multichip version of the MicroSparc CPU for flipchip bond pitch varying from 150 to 400 microns with 50 micron increments for an MCM-D technology. The MCM-D is assumed to be the MicroModule D500 merged via process[6]. A cost optimized partitioner was used to identify the partition with the lowest system cost as described in [4] (i.e. system cost = cost of IC + cost of substrate/package + cost of testing). The relative cost, size, noise, and power analysis are shown in Figures 3-7.

It is intuitively expected to have a lower system cost for lower bond pitch. This is in agreement with the cost results for 250-400 micron pitch. The reason for this trend is because lower pitch results in a higher I/O which in turn relaxes the I/O constraints for the partitioning. This allows the designs to be partitioned into smaller sets of dies which may have high I/O count. Interestingly, the cost increases as the pitch changes from 250 to 200 micron. A careful investigation reveals that the number of tracks between the pads (i.e. P_{top} in equation 2) drops from three to two for smaller pitch (assuming the substrate technology remains the same). Therefore, when the escape routing is considered, smaller P_{top} results in smaller I/O density which will constraint the partitioning from generating a lower cost partition (i.e. the number of I/Os which can be **placed** on the **die** and **routed** on the **substrate** is limited by the escape routing rather than the size of the die). For this case study and given MCM-D technology, pad pitch of 150 micron does not allow partition of the design into a meaningful set of smaller ICs.

As the bond pitch is increased, there will be more tracks allowed between the bond pads, relaxing the escape routing on the substrate. However, if the die is I/O limited, the die size will be increased resulting in a higher system cost and size. If the bond pitch is decreased, it will increase the difficulty of escape routing and limit the number of I/Os on the die. This in turn will not allow lower cost partitions based on higher I/O requirements. As the results suggest, 250 micron pitch is the lowest cost system since it balances two opposing factors: the escape routing difficulty and lower bond pitch.

As Figure 4 suggests, the system size seems to be rather flat with gradual increase in size as the pitch decreases. Smaller pitch will allow the partitioner to create smaller ICs with higher I/Os (as long as I/Os are not escape routed limited). Since there is a fixed overhead associated with each IC (such as minimum chip-to-chip spacing), the partitioning process tends to increase the overall system size.

Figures 5 and 6 show the system power consumption and relative measure of the simultaneous switching noise. Both of these metrics are directly related to the total number of I/O in the system. The lowest cost case (250 micron) is also the most power consuming and contains the highest noise level. This is because the partitioner has generated smaller sets of dies with high I/O counts.

Conclusions

Impact of bond pitch of a partitioned multichip flipchip MCM-D system has been presented for pitches varying from 150 to 400 micron. A combination of the substrate trace pitch along with bonding pitch can affect the system partitioning and therefore system cost/performance. Intuition suggest that smaller bond pitch results in a lower cost system. For this case study and given cost model , the optimum pitch is at 250 micron. Reducing the pitch below this value will not improve the system cost/performance due to the difficulties in escape routing. A different cost model or a different application may result in a different optimum bond pitch.

Acknowledgments

The MSDA (Multichip System Design Advisor) tool has been extensively used throughout this work. The authors gratefully acknowledge the contribution of the MSDA tool which was originally developed by Peter Sandborn at MCC and is now being commercialized through Savantage, Inc.

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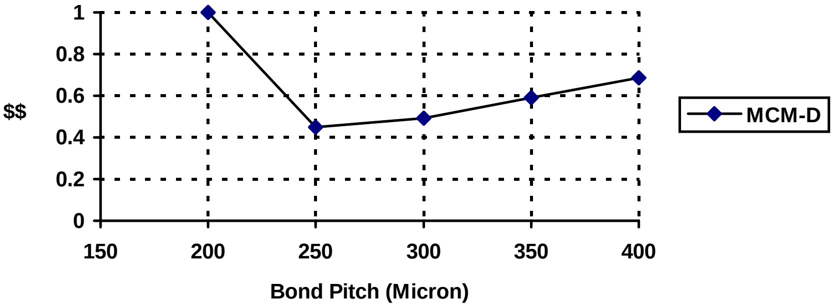

Figure 3. The Relative Comparisons of System Cost for Various Bond Pitch

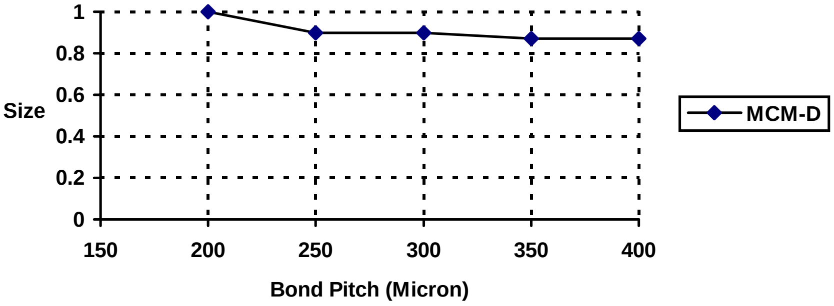

Figure 4. The Relative Comparisons of System Size for Various Bond Pitch

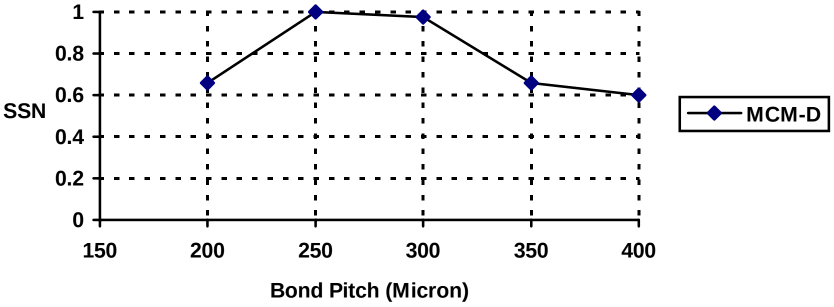

Figure 5. The Relative Comparisons of System Noise for Various Bond Pitch

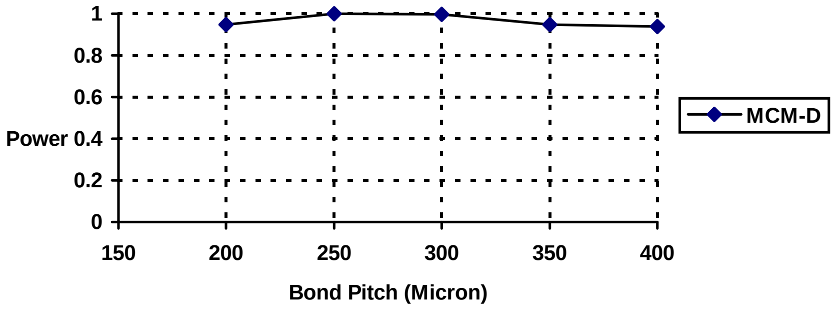

Figure 6. The Relative Comparisons of System Power for Various Bond Pitch

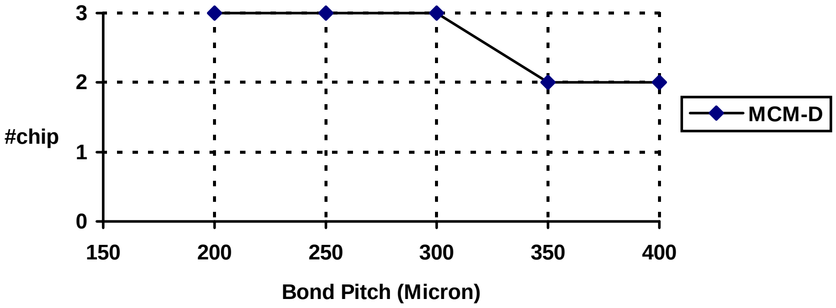

Figure 7. The Number of ICs in the Partition for Various Bond Pitch